the additional dielectric layer **21** but not through the passivation layer **22**, such that passivation layer **22** also serves as a gate insulator.

[0057] The III-N HEMT of FIG. **10** can be an enhancement-mode (i.e., normally off, with a threshold voltage greater than 0V) or a depletion-mode (i.e., normally on, with a threshold voltage less than 0V) device. Other configurations for the III-N HEMT of FIG. **10** are also possible. For example, in one implementation, the recess in the electrode-defining layer **33** only extends partially through the thickness of the electrode-defining layer **33**, such that a portion of the electrode-defining layer **33** is between the III-N materials and portion **61** of the gate (not shown). In this case, electrode-defining layer **33** can also function as a gate insulator, and it may be possible to omit the passivation layer **22** and/or the additional dielectric layer **21**. In another implementation, the recess in the electrode-defining layer **33** additionally extends through the entire thickness of the passivation layer **22**, and the gate **59** directly contacts the underlying III-N material (not shown). In yet another implementation, the recess further extends into the III-N materials (not shown), such as through the 2DEG **19**, as in the diode of FIG. **7**.

[0058] A method of forming the device of FIG. **5** is illustrated in FIGS. **11-20**. Referring to FIG. **11**, III-N material layers **11** and **12** are formed on substrate **10**, for example by metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). Passivation layer **22**, formed over the III-N material layers **11** and **12**, is then deposited by methods such as MOCVD or plasma enhanced chemical vapor deposition (PECVD). Next, as seen in FIG. **12**, a cathode contact **28** is formed which contacts the 2DEG **19** induced in the III-N material layers. Cathode contact **28** can be formed in a number of ways. For example, a metal or combination of metals can be deposited, for example by evaporation, sputtering, or CVD, in ohmic contact region **49** upon the surface of layer **12**, followed by a thermal anneal which results in the deposited metal forming a metallic alloy with the underlying semiconductor material. Alternatively, n-type dopants can be ion implanted into ohmic region **49**, followed by a metal deposition by evaporation, sputtering, or CVD, atop this region. Or the material in ohmic contact region **49** can be etched away, n-type material can be regrown in this region by MOCVD or MBE, and metal can then be deposited atop this region.

[0059] As seen in FIG. **13**, the additional dielectric layer **21** and electrode-defining layer **33** are then deposited over passivation layer **22**, for example by PECVD, sputtering, or evaporation. A recess is then etched through the electrode-defining layer, for example by reactive ion etching RIE or inductively coupled plasma (ICP) etching. The procedure for forming the recess is illustrated in FIGS. **14-19**.

[0060] Referring to FIG. **14**, a photoresist masking layer **71** is patterned on the electrode-defining **33** to have an opening **72**. Patterning can be performed by standard lithography procedures. The photoresist in the masking layer **71** is then redistributed, for example by thermally annealing the structure, resulting in the photoresist profile shown in FIG. **15**. The anneal is performed at a temperature that does not damage the photoresist layer **71** or any of the underlying layers. As illustrated in FIG. **15**, following the redistribution of the photoresist, the photoresist masking layer has slanted sidewalls **73**. The resulting profile of the photoresist layer **71** and the sidewalls **73** can be controlled by varying anneal conditions, such as anneal time, anneal temperature, and the chemistry of the ambient gas in which the anneal is performed. For example, a longer anneal time or a higher temperature may result in a smaller slope in the sidewalls **73**.

[0061] Referring to FIG. **16**, the recess in the electrode-defining layer **33** is then partially formed by performing a first etch employing an etch chemistry that etches both the photoresist in layer **71** and the material of the electrode-defining layer **33**. For example, if the electrode-defining layer **33** is SiN_x, the first etch can be performed by Reactive Ion Etching (RIE) or Inductively Coupled Plasma (ICP) etching using an etch chemistry that includes O_2 and SF_6. In some implementations, the first etch is a substantially anisotropic etch.

[0062] As illustrated in FIG. **17**, a second etch is then performed which etches the photoresist masking layer **71** without substantially etching the electrode-defining layer **33**, thereby increasing the width of the opening **72**. For example, if the electrode-defining layer **33** is SiN_x, the second etch can be performed by Reactive Ion Etching (RIE) or Inductively Coupled Plasma (ICP) etching using an etch chemistry that includes only O_2. In some implementations, the second etch is a substantially isotropic etch. A third etch is then performed which, like the first etch, utilizes an etch chemistry that etches both the photoresist in layer **71** and the material of the electrode-defining layer **33**, resulting in the profile of FIG. **18**. The photoresist etch procedure, followed by the procedure for etching both layers **71** and **33**, are then repeated multiple times, until the recess extends all the way through the electrode-defining layer **33**, resulting in the aperture having a stepped sidewall. The photoresist masking layer **71** is then removed, for example by a solvent clean, resulting in the profile shown in FIG. **19**. Additional dielectric layer **21** can be formed of a material that is not substantially etched by the etch procedure used to etch the recess in the electrode-defining layer **33**.

[0063] Referring to FIG. **20**, the portion of the additional dielectric layer **21** which is adjacent to the recess in electrode-defining layer **33** is then removed, for example by performing an etch which etches the material of the additional dielectric layer **21** but does not etch the material of electrode-defining layer **33** or passivation layer **22**. For example, when layers **33** and **22** are both SiN_x, and layer **21** is AlN, the portion of layer **21** adjacent to the recess in electrode-defining layer **33** can be chemically etched in a base, such as a photoresist developer. Next, a portion of the passivation layer **22** adjacent to the recess is etched, for example by RIE or ICP etching, resulting in the structure of FIG. **20**. Finally, electrode **39** is deposited conformally in the recess, for example by evaporation, sputtering, or CVD, and optionally the portion of layers **21** and **33** which are over the cathode contact **18** are removed, such as by chemical wet etching, or by RIE or ICP etching, resulting in the diode of FIG. **5**.

[0064] The slanted angle of the sidewalls of each step structure in the recess through the electrode-defining layer **33** results from the slanted sidewall of the photoresist masking layer **71**, as illustrated in FIG. **15**. If a vertical sidewall is desired instead of a slanted sidewall for each step structure, then the photoresist redistribution procedure described above can be omitted, or altered to change the resulting photoresist profile.

[0065] The devices of FIGS. **7-10** can be formed using slightly modified versions of the methods described above. For example, the device of FIG. **7** can be formed using the procedures described above, with one additional step. Once the recess extends through the passivation layer **22** to the